Demonstration of a Logarithmic Image Sensor with On-Chip Normal Flow Compute

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Abstract

We demonstate RECER R1 chip that has 880x480 logarithmic HDR pixels accompanied with on-chip column-parallel normal flow compute. Visitors can interact with the demo by holding and moving the RECER R1 camera, observe the results of the normal flow compute, as well as the logarithmic HDR intensity image provided by the sensor.

1. Introduction

Image sensors with on-sensor compute can be categorized to in-pixel compute that attains maximum parallelism, for example [1], or to off-array computing units within the sensor chip. In this demonstration we present RECER R1 image sensor that has 880x480 pixels and carries out on-sensor compute with a column-parallel architecture. In RECER R1 the computing is synchronized to row-wise data-readout from the array using computing circuitry that is replicated column-by-column. Also, data storage is distributed into the column circuitry so that data transfers are carried out in a column-parallel manner using local data transfers.

The RECER R1 sensor uses a regulated logarithmic pixel front-end with inherent high dynamic range (HDR) capability. Unlike integrating pixels, the regulated logarithmic pixel can be read at any time. Such a front-end is commonly used in temporal difference event cameras. The logarithmic analog pixel signal is read out to column-level delta ADCs that provide both intensity image (GS) and synchronous temporal difference events (TD EVTS), similarly to what was reported in [2]. The approach differs from circuits such as the DAVIS event image sensor in that the DAVIS does in-pixel temporal difference extraction, and provides an intensity image by integrating the pixel current [3].

RECER R1 has normal flow compute that works with the temporal difference events [4] of up to eight different timescales. The normal flow compute is carried out per-pixel in each frame. The chip also computes 8x8 thresholded normal flow pop count that allows low datarate readout and rapid reaction to changing motion patterns. In the demonstration setup the sensor is controlled with an FPGA employing a custom cycle-accurate controller, and data is provided to the host (e.g., a PC for data visualization) via USB3. The operation of the image capture and on-chip normal flow compute is demonstrated.

1.1. Chip architecture and control scheme

Figure 1 shows the chip architecture and control. The per-column delta ADCs are pitch-matched to a 9µm pixel width. The delta ADC works so that the difference of current and previous pixel value is digitized, and the difference is used to update the pixel value. Delta ADC requires a full frame memory for previous frame data. Similarly, column-level temporal difference extraction requires the previous frame. Therefore, delta ADC is a natural choice for RECER R1. The 8-bit full frame memory employs 4-level digital dynamic memory cells, while the events (11 full frames of ternary event frames are stored on chip) are stored to 3-level dynamic digital memories.

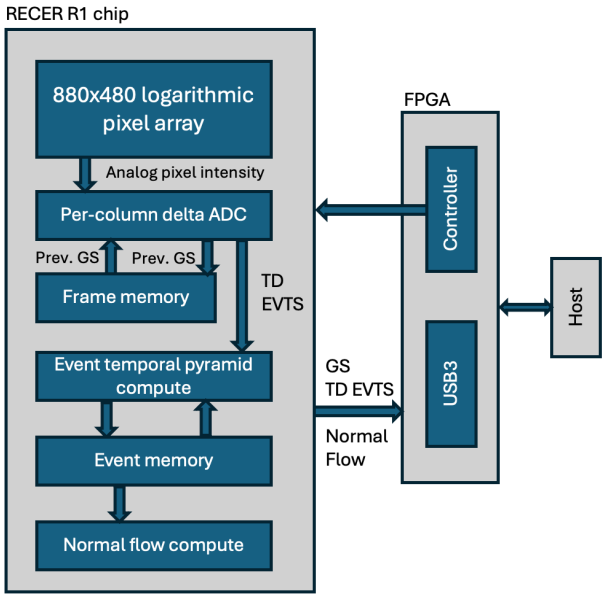

Figure 1: Chip architecture and control scheme.

Slower time-scale event frame – emulating slower rate event frame sampling – is calculated from two consecutive faster event frames using simple event arithmetic: two faster time-scale ternary event planes are summed and truncated yielding another ternary event plane that represents a 2x slower temporal difference. This is repeated so that event planes at time scales 1, 2, 4, 8, 16, 32, 64 and 128 are available, i.e., the slowest timescale events respond to 128x slower changing pixel differences as compared to the fastest events.

The resulting event planes are stored on-chip and used for normal flow compute at different timescales. Normal flow is computed using dedicated circuitry (not programmable to carry out other tasks) from two consecutive synchronously acquired event frames using simple first neighborhood event pattern comparison that detects presence and direction of moving edges [4].

In the demonstration setup we use Microsemi's Igloo 2 FPGA; the FPGA hosts a cycle-accurate custom microcontroller that is used for controlling the chip. FTDI FT600 USB3 chip is used for communication. The use of only one off-chip controller allows the image capture and on-chip compute to run at 200FPS with chip power consumption 380mW. Also, when all frame data, i.e., intensity image (120dB), temporal difference events, per-pixel normal flow and 8x8 averaged normal flow are read out, the USB bandwidth limits the speed at which the host receives data to 50FPS. Reducing data types allows faster readout, e.g., events only can be read out at 200FPS. It should be noted that the chip architecture itself allows much higher frames rates. For example, by employing multiple on-chip controllers on a similar column-parallel architecture, we have achieved >1000fps with our RECER S1 (WAFER2) chip [5].

1.2. Chip and demonstration setup details

Figure 2 shows microphotograph of the RECER R1 chip. The chip is fabricated with a 180nm CMOS and is sized at 11x9mm2. The chip is bonded to a chip carrier board (CCB) that also houses bias DACs and power regulators. The FPGA-board is on a separate PCB stacked with the CCB. The optical mount accepts C/CS-mount and M12 lenses.

Figure 3 shows example data captured with the demonstration setup. The available data types for readout are intensity image, temporal difference events, per-pixel normal flow and 8x8 normal flow. FPN correction of the raw intensity image is carried out by the host. It is possible to select which data is read out. For example, if only 8x8 normal flow is read out, amount of data transfers is at minimum. Also, data across the whole array can be read out, or only data from a region of interest (ROI). By reading out fewer data types or a smaller ROI, the FPS can be increased.

Our live demonstration will show the RECER R1 chip in operation. Visitors can interact with the demo by holding and moving the RECER R1 camera, observe the results of the normal flow compute, as well as the logarithmic HDR intensity image provided by the sensor.

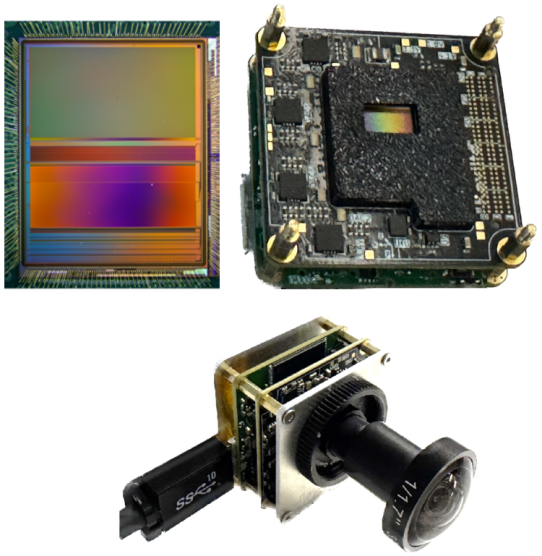

Figure 2: RECER R1 chip microphotograph, chip module (FPGA board and chip carrier board stacked) and optical/mechanical arrangement.

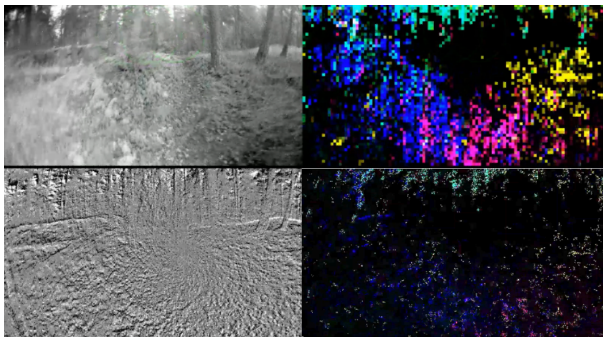

Figure 3: Example of captured data. Top left: intensity image (logarithmic image tone-mapped for viewing). Bottom left: temporal difference events, fastest event plane. Top right: 8x8 averaged normal flow. Bottom right: per-pixel per-pixel normal flow.

References

[1] SCAMP-5: S. J. Carey, A. Lopich, D. R. W. Barr, B. Wang and P. Dudek, "A 100,000 fps vision sensor with embedded 535GOPS/W 256×256 SIMD processor array," 2013 Symposium on VLSI Circuits, Kyoto, Japan, 2013, pp. C182-C183.

[2] M. Grönroos, A. Paasio and M. Laiho, "128 × 128 Pixel CMOS Event Camera With Multi-Bit Temporal Difference Event Generation," 2025 IEEE International Symposium on Circuits and Systems (ISCAS), London, United Kingdom, 2025, pp. 1-5, doi: 10.1109/ISCAS56072.2025.11043945.

[3] DAVIS: C. Brandli, R. Berner, M. Yang, S. -C. Liu and T. Delbruck, "A 240 × 180 130 dB 3 µs Latency Global Shutter Spatiotemporal Vision Sensor," in *IEEE Journal of Solid-State Circuits*, vol. 49, no. 10, pp. 2333-2341, Oct. 2014, doi: 10.1109/JSSC.2014.2342715.

[4] M. Laiho, A.Paasio, E.Lehtonen, "Apparatus for Event Stream Manipulation," WO2024213823(A1).

[5] A. Paasio et. al, "WAFER2 chip test report", https://ec.europa.eu/research/participants/documents/downloadPublic?documentIds=080166e5247751d8&appId=PPGMS